Changes Approved 4/21/05 JBF

IN THE SPECIFICATION

Please rewrite the paragraph on page 4, lines 11-15, as follows:

In Fig. 6, the number of the flip-flops that compose the scan path is set to eight only for convenience sake and for ease of description. Also, the number of flip-flops in each of the registers, which respectively comprise the flip-flops ~~101 to 103~~ 10_1 to 10_3 and the flip-flops ~~104 to 106,~~ 10_4 to 10_6 is not limited to three.

Please rewrite the paragraph beginning on page 9, line 12, and ending on page 10, line 7, as follows:

Figs. 9a, 9b, and 9c are illustrations showing timing of the test described above. Fig. 9a shows the timing of a scan mode signal, and Fig. 9b shows the timing of the clock. In an example shown in Fig. 9a, when the scan mode signal is at a high level, the semiconductor integrated circuit device is in the scan mode or in the scan-enabled state, while the scan mode signal is at a low level, the semiconductor integrated circuit device is in the normal mode or in the scan-disabled state. In an example shown in Fig. 9b, the scan clock and the clock in the normal mode are input into the same terminal. The LSI tester changes the clock period

according to whether the semiconductor integrated circuit device is in the normal mode or scans mode. In an example shown in Fig. 9c, a timing diagram for the clock in the normal mode and the scan clock input from different external terminals is shown. As shown in Fig. 9c by way of timing operations, the scan clock and the normal clock input from different external terminals are supplied to the selector of the semiconductor integrated circuit device. When the semiconductor integrated circuit device is in the scan mode, the scan clock is selected, whereas when the semiconductor integrated circuit device is in the normal mode, the normal clock is selected to be supplied to the clock input terminal CK of the flip-flop shown in Figs. ~~8 through 9.~~ 6 through 8.

Please rewrite the paragraph on page 23, lines 10-20, as follows:

Fig. 4a and 4b show a table and an illustrative circuit diagram for explaining a specific example of the path information 107 on the delay measurement path and the aggressor path. Fig. 4a is the table showing a result of extraction of the measurement path and the aggressor path (aggressor_path) in a circuit illustrated in Fig. 4b. Referring to Fig. 4b, M1 and M8 are flip-flops that

constitute a scan path. A path that extends from an output terminal Q of the flip-flop M1 to the data input terminal D of the flip-flop ~~M2~~ M8 is the measurement path. In the measurement path information, the names of the nodes that constitutes the measurement path and the transition types (rise/fall) of the signal that propagates through the measurement path are extracted.